

# WEST

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## Search Results -

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LOAD.USPT.	498753
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(34 AND (STORE NEAR9 LOAD)).USPT.	21
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## Search History

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*DB=USPT; PLUR=YES; OP=OR*

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<a href="#">L34</a>	(eliminat\$3 or avoid\$5) near5 (comput\$5 or calculat\$4) near4 address\$3	163	<a href="#">L34</a>
<a href="#">L33</a>	4633441.pn.	1	<a href="#">L33</a>
<a href="#">L32</a>	6011751.pn.	1	<a href="#">L32</a>
<a href="#">L31</a>	(store near9 load) near6 ("SAME" or identical) near4 (location\$ or address\$3)	255	<a href="#">L31</a>
<a href="#">L30</a>	(store near9 load) near9 ("SAME" or identical) near4 (location\$ or address\$3)	260	<a href="#">L30</a>
<a href="#">L29</a>	(previous\$2 or recent\$2 or last\$2) near4 (read or written or load\$3 or stor\$3) near5 address\$3 near6 (sav\$3 or restor\$3) and load near9 store	18	<a href="#">L29</a>

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<u>L27</u>	(previous\$2 or recent\$2 or last\$2) near4 (read or written or load\$3 or stor\$3) near5 address\$3 near6 (sav\$3 or restor\$3)	99	<u>L27</u>
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<u>L24</u>	5365485.pn.	1	<u>L24</u>
<u>L23</u>	address near1 cycle\$ near5 eliminat\$3	13	<u>L23</u>
<u>L22</u>	address near1 cycle\$	3533	<u>L22</u>
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<u>L20</u>	(avoid\$3 or prevent\$3 or need\$2 or eliminat\$3) near4 (comput\$5 or calculat\$3) near4 address near5 (load or store or written) near4 (previous\$2 or last\$2 or before or recent\$2)	3	<u>L20</u>
<u>L19</u>	address near4 cycle near5 (load or store or written) near4 (previous\$2 or last\$2 or before or recent\$2)	85	<u>L19</u>
<u>L18</u>	address near5 (load or store or written) near4 (previous\$2 or last\$2 or before or recent\$2)	2921	<u>L18</u>
<u>L17</u>	110 near6 (load or store or written) near6 (previous\$2 or last\$2 or before or recent\$2)	90	<u>L17</u>
<u>L16</u>	110 near6 (load or store or written)	1060	<u>L16</u>
<u>L15</u>	L13 near9 (load or store)	6	<u>L15</u>
<u>L14</u>	L13 and load and store	108	<u>L14</u>
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<u>L10</u>	address near4 cycle	12387	<u>L10</u>
<u>L9</u>	L7 and address near3 cycle	0	<u>L9</u>
<u>L8</u>	L7 and cycle	1	<u>L8</u>
<u>L7</u>	6308259.pn.	1	<u>L7</u>
<u>L6</u>	recover\$3 near5 store near3 address\$3	30	<u>L6</u>
<u>L5</u>	(sav\$3 or us\$3) near3 address near6 (written or stor\$3) near4 (previous\$3 or last\$2 or recent\$2 or before) near6 (load or store)	87	<u>L5</u>
<u>L4</u>	(sav\$3 or us\$3) near3 address near6 (written or stor\$3) near4 (previous\$3 or last\$2 or recent\$2 or before) near9 (load or store)	92	<u>L4</u>
<u>L3</u>	(sav\$3 or us\$3) near3 address near6 (written or stor\$3) near4 (previous\$3 or last\$2 or recent\$2 or before) near12 (load or store)	97	<u>L3</u>
<u>L2</u>	(sav\$3 or us\$3) near3 address near6 (written or stor\$3) near4 (previous\$3 or last\$2 or recent\$2 or before) and load and store	285	<u>L2</u>
<u>L1</u>	(sav\$3 or us\$3) near4 address near6 (written or stor\$3) near4 (previous\$3 or last\$2 or recent\$2 or before)	725	<u>L1</u>

END OF SEARCH HISTORY

**WEST**[Generate Collection](#)[Print](#)

Search Results - Record(s) 1 through 10 of 10 returned.

☐ 1. Document ID: US 6308259 B1

L7: Entry 1 of 10

File: USPT

Oct 23, 2001

US-PAT-NO: 6308259

DOCUMENT-IDENTIFIER: US 6308259 B1

TITLE: Instruction queue evaluating dependency vector in portions during different clock phases

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
Draw Desc	Image									

☐ 2. Document ID: US 6216200 B1

L7: Entry 2 of 10

File: USPT

Apr 10, 2001

US-PAT-NO: 6216200

DOCUMENT-IDENTIFIER: US 6216200 B1

TITLE: Address queue

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
Draw Desc	Image									

☐ 3. Document ID: US 6212623 B1

L7: Entry 3 of 10

File: USPT

Apr 3, 2001

US-PAT-NO: 6212623

DOCUMENT-IDENTIFIER: US 6212623 B1

TITLE: Universal dependency vector/queue entry

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
Draw Desc	Image									

☐ 4. Document ID: US 6212622 B1

L7: Entry 4 of 10

File: USPT

Apr 3, 2001

US-PAT-NO: 6212622

DOCUMENT-IDENTIFIER: US 6212622 B1

TITLE: Mechanism for load block on store address generation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 5. Document ID: US 6141747 A

L7: Entry 5 of 10

File: USPT

Oct 31, 2000

US-PAT-NO: 6141747

DOCUMENT-IDENTIFIER: US 6141747 A

TITLE: System for store to load forwarding of individual bytes from separate store buffer entries to form a single load word

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 6. Document ID: US 6122727 A

L7: Entry 6 of 10

File: USPT

Sep 19, 2000

US-PAT-NO: 6122727

DOCUMENT-IDENTIFIER: US 6122727 A

TITLE: Symmetrical instructions queue for high clock frequency scheduling

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 7. Document ID: US 6108770 A

L7: Entry 7 of 10

File: USPT

Aug 22, 2000

US-PAT-NO: 6108770

DOCUMENT-IDENTIFIER: US 6108770 A

TITLE: Method and apparatus for predicting memory dependence using store sets

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 8. Document ID: US 5841998 A

L7: Entry 8 of 10

File: USPT

Nov 24, 1998

US-PAT-NO: 5841998

DOCUMENT-IDENTIFIER: US 5841998 A

TITLE: System and method of processing instructions for a processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 9. Document ID: US 5475823 A

L7: Entry 9 of 10

File: USPT

Dec 12, 1995

US-PAT-NO: 5475823

DOCUMENT-IDENTIFIER: US 5475823 A

TITLE: Memory processor that prevents errors when load instructions are moved in the execution sequence

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 10. Document ID: US 4992938 A

L7: Entry 10 of 10

File: USPT

Feb 12, 1991

US-PAT-NO: 4992938

DOCUMENT-IDENTIFIER: US 4992938 A

TITLE: Instruction control mechanism for a computing system with register renaming, map table and queues indicating available registers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

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Term	Documents
PIPELIN\$5	0
PIPELIN.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	25
PIPELINABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	14
PIPELINCD.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
PIPELIND.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	3
PIPELINE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	96557
PIPELINEA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
PIPELINEABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	78
PIPELINEAND.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	3
PIPELINEB.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	13
PIPELINECAN.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
(L5 AND PIPELIN\$5).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	10

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**WEST**

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L7: Entry 9 of 10

File: USPT

Dec 12, 1995

DOCUMENT-IDENTIFIER: US 5475823 A

TITLE: Memory processor that prevents errors when load instructions are moved in the execution sequence

Abstract Text (1):

A memory processor which prevents errors when the compiler advances long latency load instructions in the instruction sequence to reduce the loss of efficiency resulting from the latency time. The memory processor intercepts all load and store instructions prior to the instructions entering the memory pipeline. The memory processor stores load instructions for a period of time sufficient to determine if any subsequent store instruction that would have been executed prior to the load instruction, had the load instruction not been moved, references the same address as that specified in the load instruction. If a store instruction references the load instruction address, the invention returns the same data as the load instruction would have if it was not moved by the compiler.

Detailed Description Text (2):

The present invention effectively separates the time when the address (and other parameters) of a load instruction is presented to a memory and the time at which the load instruction effectively samples the state of the memory. In prior art systems, the time that the address of a load instruction is presented to the memory is also the time that the load effectively samples the state of the memory. This is also the time that the load is said to be "executed". Even in pipelined memory systems in which load instructions physically sample the state of the memory a number of cycles after the load instruction is issued, the memory is effectively sampled at the instant that the load is issued because the data returned by the load captures all those memory state modification perpetrated by operations issued before the load. This is true even if these operations have not physically updated the memory by the time the load is issued.

Detailed Description Text (5):

When used in conjunction with the present invention, a "watch-window" is defined for each load instruction that is moved by the compiler. In one embodiment of the present invention, the compiler stores a count in each long latency load instruction that indicates the number of instructions over which it was moved with respect to the code ordering implied in the original program. The present invention detects such load instructions as they enter the memory pipeline and stores information specifying the load instruction and the number of instructions over which it was moved. Denote the number of instructions over which the long latency load instruction was moved by N. On each of the following N instruction cycles, the present invention examines the instructions entering the memory pipeline to determine if the instruction in question is a store instruction referencing the same memory location as that specified in the load instruction. If no such store instruction is detected, the load instruction in question will return valid data and no action need be taken. If, however, a store instruction referencing the memory location in question was detected during the N instruction cycles, the present invention causes the long latency load instruction to be re-executed at the location in the code sequence at which it would have been executed without the move. During this re-execution, the present invention signals the CPU to suspend operations for the latency time of the load instruction in question.

Detailed Description Text (17):

The embodiments of the present invention described above cause a load instruction

whose address has been used in a store instruction during the watch window to be re-issued at the point in the code sequence that the load instruction would have been issued had the load instruction not been moved by the compiler. An alternative mechanism for dealing with this situation is to provide a data forwarding system. A block diagram of memory processor 510 according to the present invention which utilizes such a data forwarder is illustrated in FIGS. 5 and 6. As was the case with the previously described embodiments of the present invention, memory processor 510 detects load and store instructions communicated by a CPU 516 to a memory 512. The instructions are detected by instruction detector 520 which recognizes load instructions that have been advanced in the instruction sequence by the compiler. Information specifying the load instruction is logged in a register file 522 as described above with reference to memory processor 10. Information specifying the load instruction addresses is also logged in a data forwarding circuit 550. The load instruction proceeds to query memory 512 and the corresponding memory data is returned to data forwarder 550 at the end of the latency period. The data may also be returned directly to the register file in CPU 516. Address comparator 528 compares the addresses of all store instructions with the addresses of the load instructions stored in register file 522 to check for partial or complete overlap of the memory locations accessed by the load and store instructions. If a store instruction overwrites part or all of the data accessed by the load instruction, controller 524 sets the flag corresponding to the load instruction in question.

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Search Results - Record(s) 1 through 20 of 38 returned.

☐ 1. Document ID: US 6477640 B1

L3: Entry 1 of 38

File: USPT

Nov 5, 2002

US-PAT-NO: 6477640

DOCUMENT-IDENTIFIER: US 6477640 B1

TITLE: Apparatus and method for predicting multiple branches and performing out-of-order branch resolution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw. Desc	Image										

☐ 2. Document ID: US 6269436 B1

L3: Entry 2 of 38

File: USPT

Jul 31, 2001

US-PAT-NO: 6269436

DOCUMENT-IDENTIFIER: US 6269436 B1

TITLE: Superscalar microprocessor configured to predict return addresses from a return stack storage

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw. Desc	Image										

☐ 3. Document ID: US 6247124 B1

L3: Entry 3 of 38

File: USPT

Jun 12, 2001

US-PAT-NO: 6247124

DOCUMENT-IDENTIFIER: US 6247124 B1

TITLE: Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw. Desc	Image									

☐ 4. Document ID: US 6189087 B1

L3: Entry 4 of 38

File: USPT

Feb 13, 2001

US-PAT-NO: 6189087

DOCUMENT-IDENTIFIER: US 6189087 B1



TITLE: Superscalar instruction decoder including an instruction queue

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

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☐ 5. Document ID: US 6157998 A

L3: Entry 5 of 38

File: USPT

Dec 5, 2000

US-PAT-NO: 6157998

DOCUMENT-IDENTIFIER: US 6157998 A

TITLE: Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

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☐ 6. Document ID: US 6085233 A

L3: Entry 6 of 38

File: USPT

Jul 4, 2000

US-PAT-NO: 6085233

DOCUMENT-IDENTIFIER: US 6085233 A

TITLE: System and method for cellular network computing and communications

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

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☐ 7. Document ID: US 6070235 A

L3: Entry 7 of 38

File: USPT

May 30, 2000

US-PAT-NO: 6070235

DOCUMENT-IDENTIFIER: US 6070235 A

TITLE: Data processing system and method for capturing history buffer data

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

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☐ 8. Document ID: US 6061710 A

L3: Entry 8 of 38

File: USPT

May 9, 2000

US-PAT-NO: 6061710

DOCUMENT-IDENTIFIER: US 6061710 A

TITLE: Multithreaded processor incorporating a thread latch register for interrupt service new pending threads

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 9. Document ID: US 6052708 A

L3: Entry 9 of 38

File: USPT

Apr 18, 2000

US-PAT-NO: 6052708

DOCUMENT-IDENTIFIER: US 6052708 A

TITLE: Performance monitoring of thread switch events in a multithreaded processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 10. Document ID: US 6035393 A

L3: Entry 10 of 38

File: USPT

Mar 7, 2000

US-PAT-NO: 6035393

DOCUMENT-IDENTIFIER: US 6035393 A

TITLE: Stalling predicted prefetch to memory location identified as uncacheable using dummy stall instruction until branch speculation resolution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 11. Document ID: US 6014734 A

L3: Entry 11 of 38

File: USPT

Jan 11, 2000

US-PAT-NO: 6014734

DOCUMENT-IDENTIFIER: US 6014734 A

TITLE: Superscalar microprocessor configured to predict return addresses from a return stack storage

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 12. Document ID: US 5974535 A

L3: Entry 12 of 38

File: USPT

Oct 26, 1999

US-PAT-NO: 5974535

DOCUMENT-IDENTIFIER: US 5974535 A

TITLE: Method and system in data processing system of permitting concurrent processing of instructions of a particular type

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K/MC

☐ 13. Document ID: US 5974240 A

L3: Entry 13 of 38

File: USPT

Oct 26, 1999

US-PAT-NO: 5974240

DOCUMENT-IDENTIFIER: US 5974240 A

TITLE: Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K/MC

☐ 14. Document ID: US 5964869 A

L3: Entry 14 of 38

File: USPT

Oct 12, 1999

US-PAT-NO: 5964869

DOCUMENT-IDENTIFIER: US 5964869 A

TITLE: Instruction fetch mechanism with simultaneous prediction of control-flow instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K/MC

☐ 15. Document ID: US 5954815 A

L3: Entry 15 of 38

File: USPT

Sep 21, 1999

US-PAT-NO: 5954815

DOCUMENT-IDENTIFIER: US 5954815 A

TITLE: Invalidating instructions in fetched instruction blocks upon predicted two-step branch operations with second operation relative target address

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

K/MC

☐ 16. Document ID: US 5935238 A

L3: Entry 16 of 38

File: USPT

Aug 10, 1999

US-PAT-NO: 5935238

DOCUMENT-IDENTIFIER: US 5935238 A

TITLE: Selection from multiple fetch addresses generated concurrently including predicted and actual target by control-flow instructions in current and previous instruction bundles

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 17. Document ID: US 5881278 A

L3: Entry 17 of 38

File: USPT

Mar 9, 1999

US-PAT-NO: 5881278

DOCUMENT-IDENTIFIER: US 5881278 A

TITLE: Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 18. Document ID: US 5870612 A

L3: Entry 18 of 38

File: USPT

Feb 9, 1999

US-PAT-NO: 5870612

DOCUMENT-IDENTIFIER: US 5870612 A

TITLE: Method and apparatus for condensed history buffer

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 19. Document ID: US 5864707 A

L3: Entry 19 of 38

File: USPT

Jan 26, 1999

US-PAT-NO: 5864707

DOCUMENT-IDENTIFIER: US 5864707 A

TITLE: Superscalar microprocessor configured to predict return addresses from a return stack storage

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 20. Document ID: US 5860014 A

L3: Entry 20 of 38

File: USPT

Jan 12, 1999

US-PAT-NO: 5860014

DOCUMENT-IDENTIFIER: US 5860014 A

TITLE: Method and apparatus for improved recovery of processor state using history buffer

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw	Desc	Image							

KWC

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Term	Documents
DEPENDENT.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	537668
DEPENDENTS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	436
DEPENDENC\$3	0
DEPENDENC.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	6
DEPENDENCC.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
DEPENDENCD.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
DEPENDENCE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	138537
DEPENDENCEAT.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
DEPENDENCED.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
DEPENDENCEN.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
DEPENDENCEOF.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	3
((DEPENDENC\$3 OR DEPENDENT) AND L2).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	38

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Search Results - Record(s) 21 through 38 of 38 returned.

☐ 21. Document ID: US 5857089 A

L3: Entry 21 of 38

File: USPT

Jan 5, 1999

US-PAT-NO: 5857089

DOCUMENT-IDENTIFIER: US 5857089 A

TITLE: Floating point stack and exchange instruction

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw. Desc	Image									

☐ 22. Document ID: US 5850542 A

L3: Entry 22 of 38

File: USPT

Dec 15, 1998

US-PAT-NO: 5850542

DOCUMENT-IDENTIFIER: US 5850542 A

TITLE: Microprocessor instruction hedge-fetching in a multiprediction branch environment

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw. Desc	Image									

☐ 23. Document ID: US 5841999 A

L3: Entry 23 of 38

File: USPT

Nov 24, 1998

US-PAT-NO: 5841999

DOCUMENT-IDENTIFIER: US 5841999 A

TITLE: Information handling system having a register remap structure using a content addressable table

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw. Desc	Image									

☐ 24. Document ID: US 5822575 A

L3: Entry 24 of 38

File: USPT

Oct 13, 1998

US-PAT-NO: 5822575

DOCUMENT-IDENTIFIER: US 5822575 A

TITLE: Branch prediction storage for storing branch prediction information such that

a corresponding tag may be routed with the branch instruction

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 25. Document ID: US 5805876 A

L3: Entry 25 of 38

File: USPT

Sep 8, 1998

US-PAT-NO: 5805876

DOCUMENT-IDENTIFIER: US 5805876 A

TITLE: Method and system for reducing average branch resolution time and effective misprediction penalty in a processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 26. Document ID: US 5796974 A

L3: Entry 26 of 38

File: USPT

Aug 18, 1998

US-PAT-NO: 5796974

DOCUMENT-IDENTIFIER: US 5796974 A

TITLE: Microcode patching apparatus and method

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 27. Document ID: US 5796973 A

L3: Entry 27 of 38

File: USPT

Aug 18, 1998

US-PAT-NO: 5796973

DOCUMENT-IDENTIFIER: US 5796973 A

TITLE: Method and apparatus for decoding one or more complex instructions into concurrently dispatched simple instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 28. Document ID: US 5784603 A

L3: Entry 28 of 38

File: USPT

Jul 21, 1998

US-PAT-NO: 5784603

DOCUMENT-IDENTIFIER: US 5784603 A

TITLE: Fast handling of branch delay slots on mispredicted branches

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

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☐ 29. Document ID: US 5748935 A

L3: Entry 29 of 38

File: USPT

May 5, 1998

US-PAT-NO: 5748935

DOCUMENT-IDENTIFIER: US 5748935 A

TITLE: Reconstruction of young bits in annex after mispredicted execution branch in pipelined processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 30. Document ID: US 5696955 A

L3: Entry 30 of 38

File: USPT

Dec 9, 1997

US-PAT-NO: 5696955

DOCUMENT-IDENTIFIER: US 5696955 A

TITLE: Floating point stack and exchange instruction

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 31. Document ID: US 5634103 A

L3: Entry 31 of 38

File: USPT

May 27, 1997

US-PAT-NO: 5634103

DOCUMENT-IDENTIFIER: US 5634103 A

TITLE: Method and system for minimizing branch misprediction penalties within a processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC

☐ 32. Document ID: US 5604909 A

L3: Entry 32 of 38

File: USPT

Feb 18, 1997

US-PAT-NO: 5604909

DOCUMENT-IDENTIFIER: US 5604909 A

TITLE: Apparatus for processing instructions in a computing system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KVMC



Jul 9, 1996



Sep 12, 1995

KONE

Feb 15, 1994



Jun 30, 1992

K000C

☐ 37. Document ID: US 3969723 A

L3: Entry 37 of 38

File: USPT

Jul 13, 1976

US-PAT-NO: 3969723

DOCUMENT-IDENTIFIER: US 3969723 A

TITLE: On-line modification of computer programs

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Drawn Desc	Image								

KMC

☐ 38. Document ID: US 3969722 A

L3: Entry 38 of 38

File: USPT

Jul 13, 1976

US-PAT-NO: 3969722

DOCUMENT-IDENTIFIER: US 3969722 A

TITLE: Method and apparatus for operator interrogation of simulated control circuits

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Drawn Desc	Image								

KMC

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